National Semiconductor

May 2001

CLC520
Amplifier with Voltage Controlled Gain, AGC +Amp

General Description

The CLC520 is a wideband DC-coupled amplifier with voltage controlled gain (AGC). The amplifier has a high impedance, differential signal input; a high bandwidth, gain control input; and a single-ended voltage output. Signal channel performance is outstanding with 160MHz small signal bandwidth, 0.5 degree linear phase deviation (to 60MHz) and 0.04% signal nonlinearity at $4V_{PP}$ output.

Gain control is very flexible and easy to use. Maximum gain may be set over a nominal range of 2 to 100 with one external resistor. In addition, the gain control input provides more than 40dB of voltage controlled gain adjustment from the maximum gain setting. For example, a CLC520 may be set for a maximum gain of 2 (or 6dB) for a voltage controlled gain range from 40dB to less than 34dB. Alternatively, the CLC520 could be set for a maximum gain of 100 or (40dB) for a voltage controlled gain range from 40dB to less than 0dB.

The gain control bandwidth of 100MHz is superb for AGC/ALC loop stabilization. And since the gain is minimum with a zero volt input and maximum with a +2 volt input, driving the control input is easy.

Finally, the CLC520 differential inputs, and ground referenced voltage output take the trouble out of designing DC-coupled AGC circuits for display normalizers; signal leveling automatic circuits; etc.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-91694

Space level versions also available.

For more information, visit http://www.national.com/mil

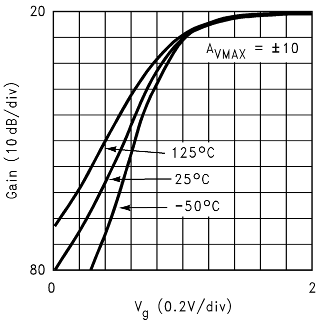
Features

- 160MHz, −3dB bandwidth
- 2000V/µsec slew rate
- 0.04% signal nonlinearity at $4V_{PP}$ output
- −43dB feedthrough at 30MHz
- User adjustable gain range
- Differential voltage input and single-ended voltage output

Applications

- Wide bandwidth AGC systems
- Automatic signal leveling
- Video signal processing
- Voltage controlled filters
- Differential amplifier
- Amplitude modulation

Gain vs. V_g



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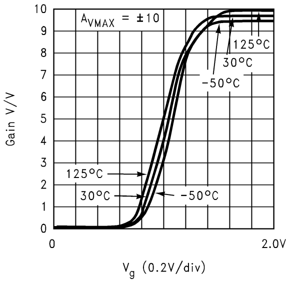

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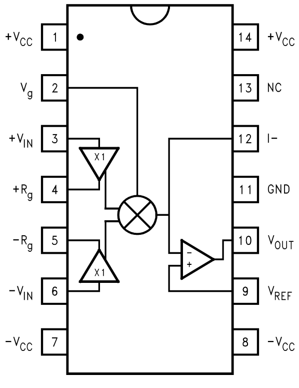
Gain vs. V_g

Connection Diagram



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Pinout
DIP & SOIC

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Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
14-pin plastic DIP	−40˚C to +85˚C	CLC520AJP	CLC520AJP	N14A
14-pin plastic SOIC	−40˚C to +85˚C	CLC520AJE	CLC520AJE	M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	±7V
I_{OUT} Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	60mA
Common Mode Input Voltage	±V_{CC}
V_{IN} Differential Input Voltage	10V
V_g Differential Input Voltage	±V_{CC}
V_{ref} Differential Input Voltage	±V_{CC}
Junction Temperature	+150˚C
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec
ESD (human body model)	500V

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	55˚C/W	105˚C/W
SOIC	45˚C/W	120˚C/W

Electrical Characteristics

A_V = +10, V_{CC} = ±5V, R_L = 100Ω, R_f = 1kΩ, R_g = 182Ω, V_g = +2V; unless specified

Symbol	**Parameter**	**Conditions**	**Typ**	**Max/Min** (Note 2)			**Units**
Ambient Temperature		CLC520AJ	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	V_{OUT} <0.5V_{PP}	160	>110	>120	>120	MHz
SSBW		V_{OUT} <0.5V_{PP} (AJE only)	140	>90	>100	>100	MHz
LSBW		V_{OUT}<4.0V_{PP}	140	>85	>100	>100	MHz
	-3dB Bandwidth	V_{OUT} <0.5V_{PP}					
SBWC	Gain Control Channel	V_{IN} = +0.2V, V_g = +1VDC	100	>80	>80	>80	MHz
	Gain Flatness	V_{OUT}< 0.5V_{PP}					
GFPL	Peaking	0.1MHz to 30MHz	0	<0.4	<0.3	<0.4	dB
GFPH	Peaking	0.1MHz to 20MHz	0	<0.7	<0.5	<0.7	dB
GFRL	Rolloff	0.1MHz to 30MHz	0.1	<0.4	<0.3	<0.4	dB
GFRH	Rolloff	0.1MHz to 60MHz	0.5	<1.3	<1	<1.3	dB
LPD	Linear Phase Deviation	0.1MHz to 60MHz	0.5	<1.2	<1	<1.2	deg
FDTH	Feedthrough	V_g = 0V, V_{IN} = -22dBm	-38	<-31	<-31	<-31	dB
TRS	Rise and Fall Time	0.5V Step	2.5	<3.7	<3	<3	ns
TRL		4.0V Step	3.7	<5	<5	<5	ns
TS	Settling Time to ±0.1%	2.0V Step	12	<18	<18	<18	ns
OS	Overshoot	0.5V Step	0	<15	<15	<15	%
SR	Slew Rate	4V Step	2000	>1450	>1450	>1450	V/µsec
HD2	2nd Harmonic Distortion	2V_{PP}, 20MHz	−47	<−40	<−40	<−35	dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 20MHz	−60	<−50	<−50	<−45	dBc
	Equivalent Output Noise	(÷10 for input noise) (Note 3)					
SNF	Noise floor	1MHz to 200MHz	−132	<−130	<−130	<−129	dBm (1Hz)
INV	Integrated noise	1MHz to 200MHz	800	<1000	<1000	<1100	µV
DG	Differential Gain (Note 4)	at 3.58MHz	0.15				%
DP	Differential Plase (Note 4)	at 3.58MHz	0.15				deg
Static, DC Performance							
SGNL	Integral Signal Nonlinearity	V_{OUT} = 4V_{PP}	0.04	<0.1	<0.1	<0.2	%
	Gain Accuracy	R_f = 1kΩ, R_g = 182Ω					
GACCU	For Nominal Max Gain = 20dB		±0	<±1.0	<±0.5	<±0.5	dB
VOS	Output Offset Voltage (Note 5)		40	<150	<120	<150	mV
DVOS	Average Temperature Coefficient		100	<400	–	<300	µV/˚C

Electrical Characteristics (Continued)

A_V = +10, V_{CC} = ±5V, R_L = 100Ω, R_f = 1kΩ, R_g = 182Ω, V_g = +2V; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min (Note 2)			Units
IB	Input Bias Current (Note 5)		12	<61	<28	<28	µA
DIB	Average Temperature Doefficient		100	<415	-	<165	nA/°C
IOS	Input Offset Current		0.5	<4	<2	<2	µA
DIOS	Average Temperature Coefficient		5	<40	-	<20	nA/°C
PSS	Power Supply Sensitivity	Output Referred DC	10	<28	<28	<28	mV/V
CMRR	Common Mode Rejection Ratio	Input Referred	70	>59	>59	>59	dB
ICC	Supply Current (Note 5)	No Load	28	<38	<38	<38	mA
RIN	V_{IN} Signal Input	Resistance	200	>50	>100	>100	kΩ
CIN		Capacitance	1	<2	<2	<2	pF
DMIR	V_{IN} Differential Voltage Range	R_g = 182Ω only	±280	±250	±250	±210	mV
CMIR	Common Mode Voltage Range		±2.2	>±1.4	>±2	>±2	V
RINC	V_g Control Input	Resistance	750	>535	>600	>600	Ω
CINC		Capacitance	1	<2	<2	<2	pF
VGHI	V_g Input Voltage	For Max Gain	1.6	<2	<2	<2	kΩ
VGLO		For Min Gain	0.4	>0	>0	>0	V
RO	Output Impedance	At DC	0.1	<0.3	<0.2	<0.2	Ω
VO	Output Voltage Range	No Load	±3.5	>±3	>±3.2	>±3.2	V
IO	Output Current		±60	>±35	>±50	>±50	mA

Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Note 2: Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: Measured at A_{VMAX} = 10, V_g = +2V

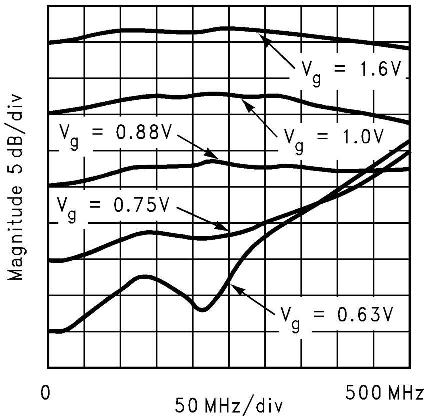
Note 4: Differential gain and phase are measured at: A_V = +20, V_g = +2V, R_L = 150Ω, R_f = 2kΩ, R_g = 182Ω, equivalent video signal of 0-100 IRE with 40 IRE_{PP} at 3.58 MHz.

Note 5: AJ-level: spec. is 100% tested at +25°C.

Typical Performance Characteristics

(T_A = 25˚C, A_V = +10, V_{CC} = ±5V, R_L = 100Ω, R_f = 1kΩ, R_g = 182Ω, V_g = +2V)

Frequency Response, A_{VMAX} = ± 2



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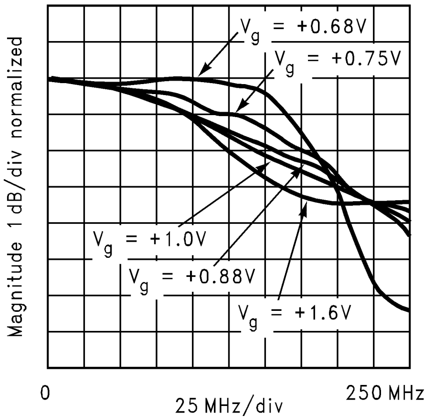
Frequency Response, A_{VMAX} = ± 10



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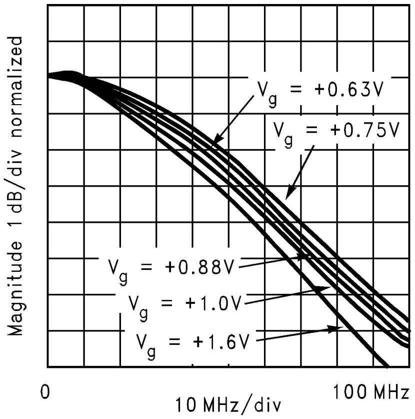
Frequency Response, A_{VMAX} = ±100



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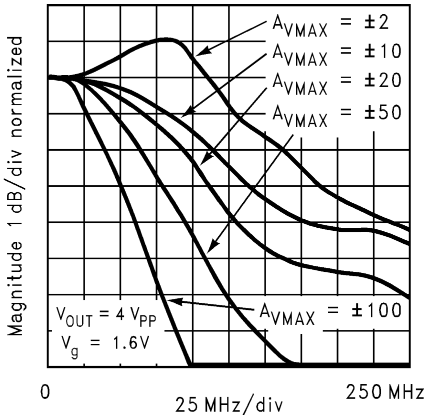
Large Signal Frequency Response



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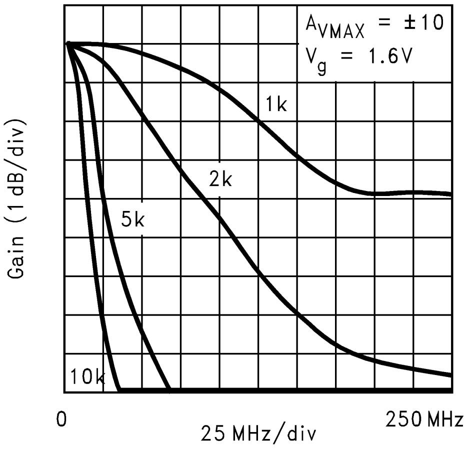
Small Signal Gain vs. R_f



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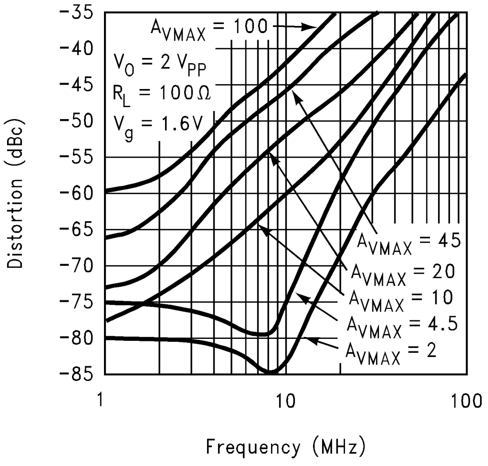
2nd Harmonic Distortion



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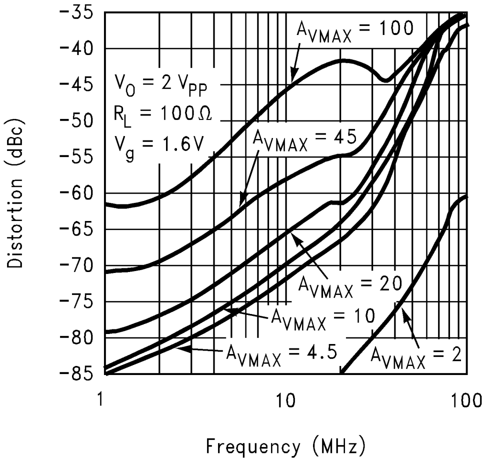
Typical Performance Characteristics (T_A = 25°C, A_V = +10, V_{CC} = ±5V, R_L = 100Ω, R_f = 1kΩ, R_g = 182Ω, V_g = +2V) (Continued)

3rd Harmonic Distortion



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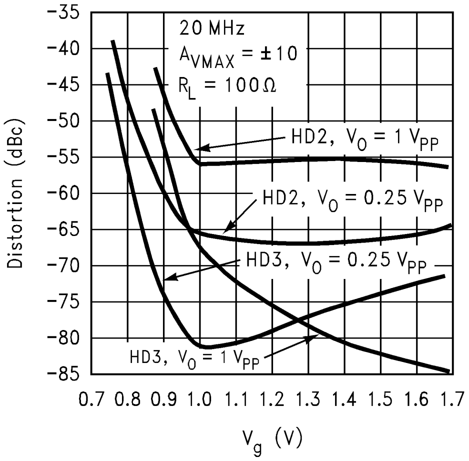
2nd and 3rd Harmonic Distortion vs. V_g



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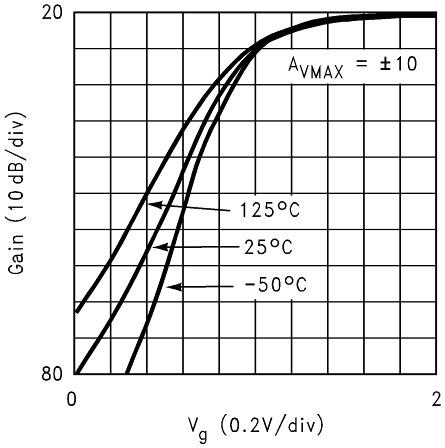
Gain vs. V_g



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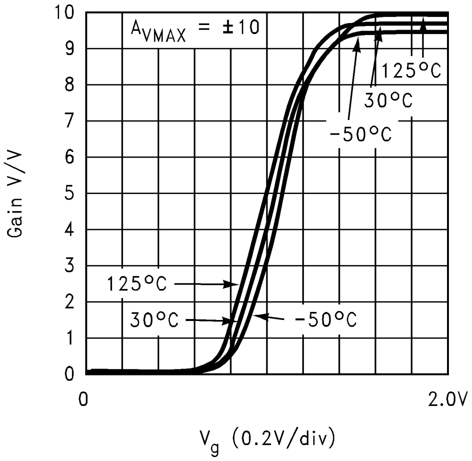
Gain vs. V_g



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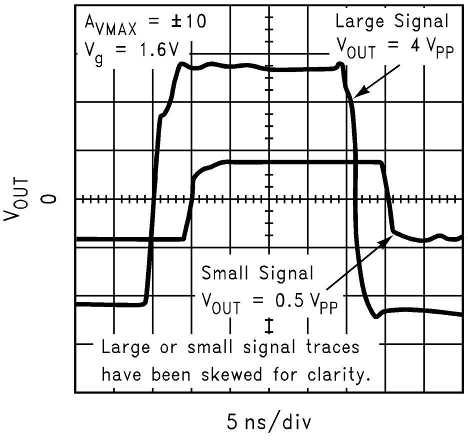
Large and Small Signal Pulse Response



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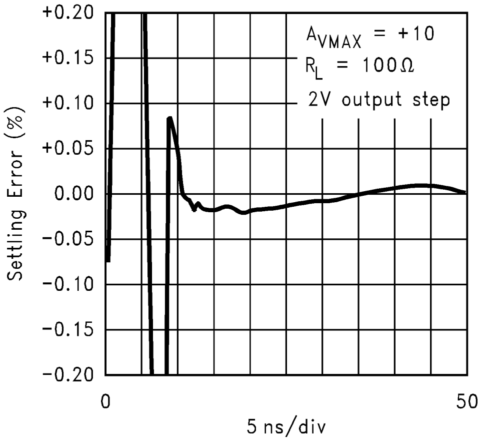
Settling Time, V_g = 2V



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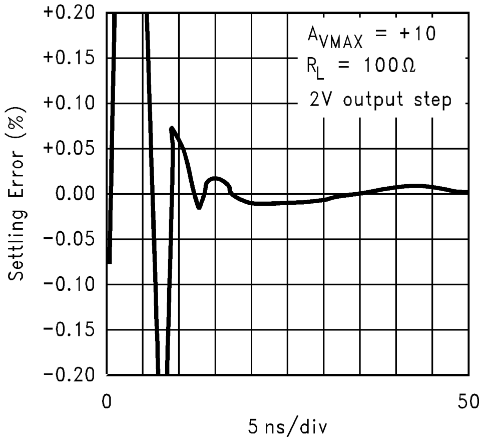
Typical Performance Characteristics (T_A = 25˚C, A_V = +10, V_{CC} = ±5V, R_L = 100Ω, R_f = 1kΩ, R_g = 182Ω, V_g = +2V) (Continued)

Settling Time, V_g = 1.2V



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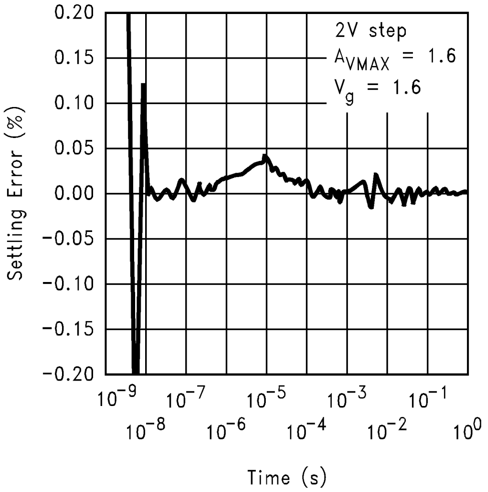
Long-Term Settling Time



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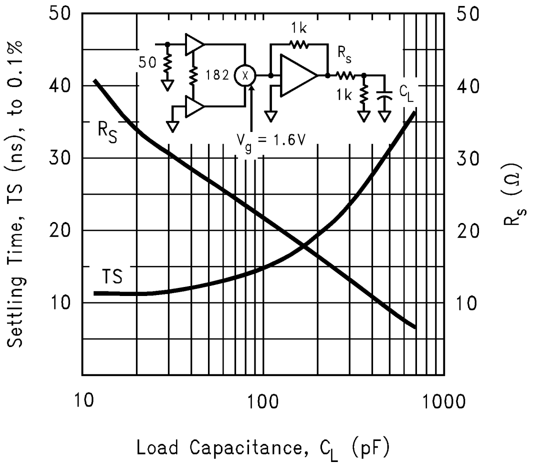
Settling Time vs. Capacitive Load, A_{VMAX} = ±10



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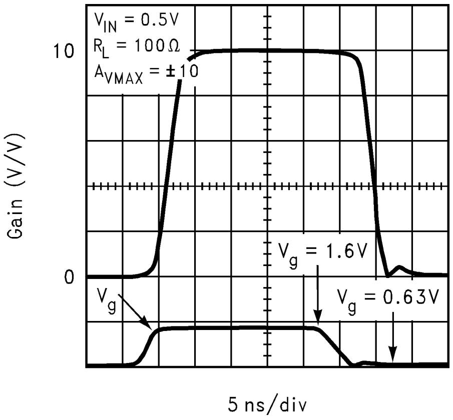
Gain Control Settling Time



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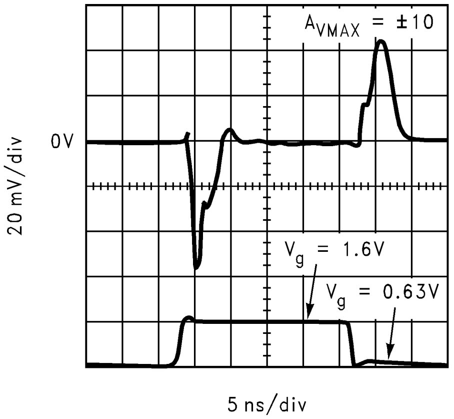
Gain Control Channel Feedthrough



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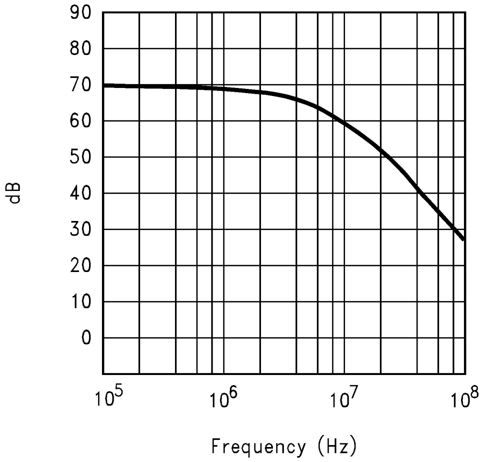
CMRR



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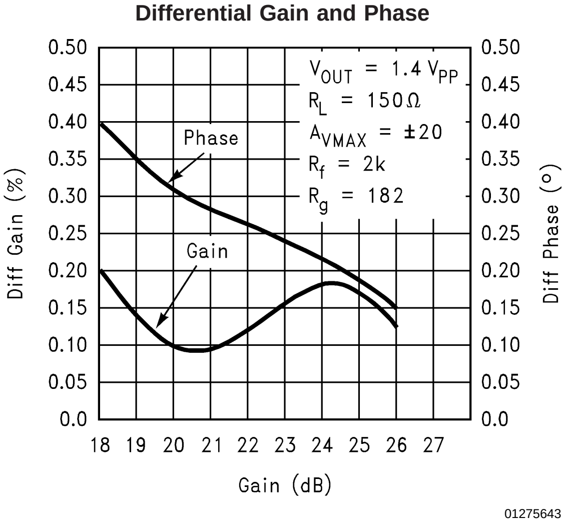
Typical Performance Characteristics (T_A = 25°C, A_V = +10, V_{CC} = ±5V, R_L = 100Ω, R_f = 1kΩ, R_g = 182Ω, V_g = +2V) (Continued)


Differential Gain and Phase

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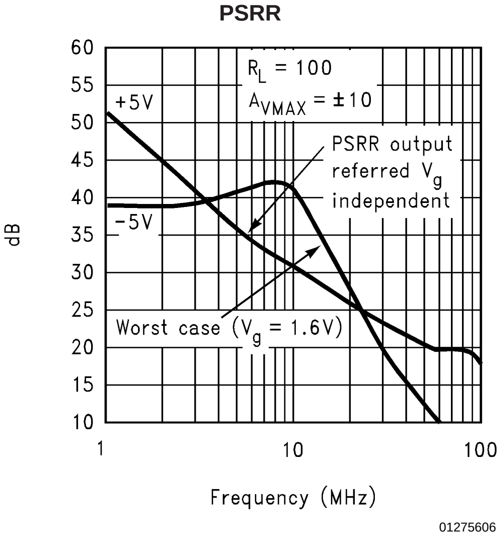
PSRR

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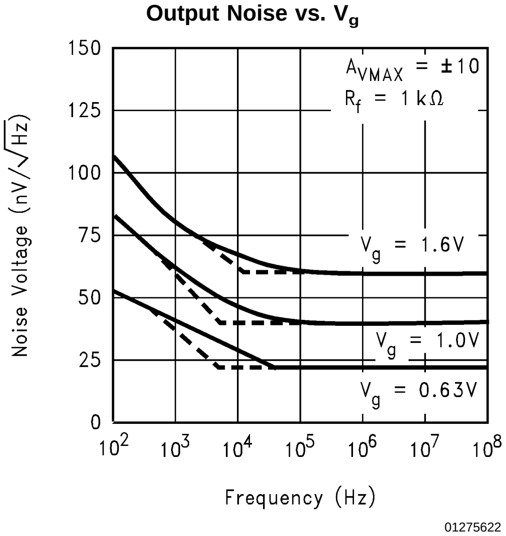
Output Noise vs. V_g

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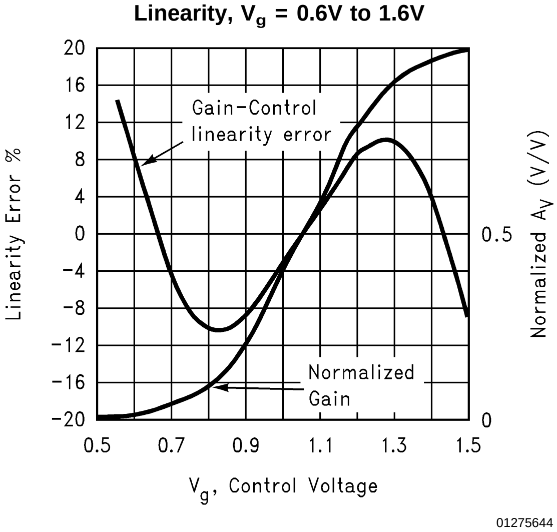
Linearity, V_g = 0.6V to 1.6V

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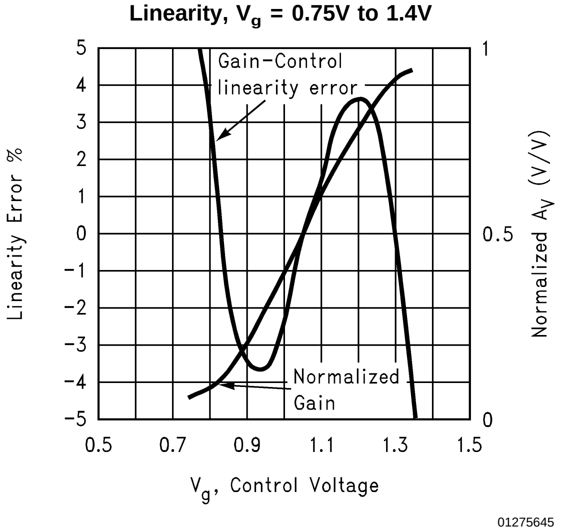
Linearity, V_g = 0.75V to 1.4V

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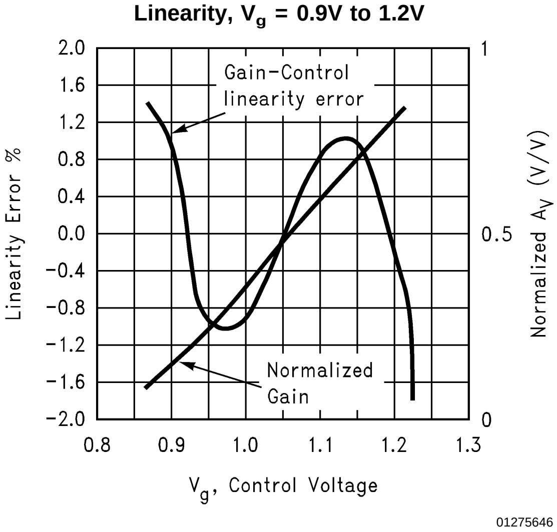
Linearity, V_g = 0.9V to 1.2V

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Application Information

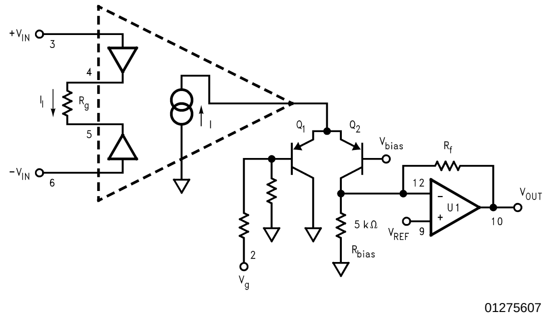


FIGURE 1. CLC520 Simplified Schematic

Simplified Circuit Description

A simplified schematic for the CLC520 is given in *Figure 1*. $+V_{IN}$ and $-V_{IN}$ are buffered with closed-loop voltage followers inducing a signal current in R_g proportional to $(+V_{IN})-(-V_{IN})$, the differential input voltage. This current controls a current source which supplies two well matched transistors, Q1 and Q2.

The current flowing through Q2 is converted to the final output voltage using R_f and output amplifier, U1. By changing the fraction of the signal current I which flows through Q2 the gain is changed. This is done by changing the voltage applied differentially to the bases of Q1 and Q2. For example, with V_g = 0, Q1 is on and Q2 is off. With zero signal current of flowing through Q2 into R_f, the CLC520 is set to minimum gain. Conversely, with V_g = 2V, Q1 is off and all of the signal current I flows through Q2 to R_f producing maximum gain. With V_g set to 1.1V, the bases of Q1 and Q2 are set to approximately the same voltage, causing their collector currents to equally divide the signal current I, and establish the gain at one half the maximum gain.

Typical application circuit

Figure 2 illustrates a voltage-controlled gain block offering broadband performance in a 50Ω system environment. The input signal is applied to pin 3 of the CLC520 and terminating resistor R2. Gain control signals are applied to pin 2. The net gain control port input impedance is 50Ω, set by the parallel combination of R1 and the 750Ω input impedance of pin 2 of the CLC520. R_f is set to the standard value, 1kΩ, and R_g sets the maximum voltage gain to 10V/V. Output impedance is set by R_o to 50Ω so with 50Ω source and load terminations, the gain is approximately 14dB.

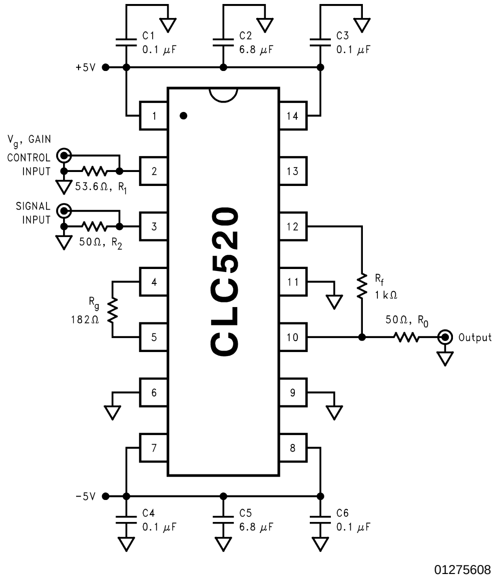


FIGURE 2. CLC520 Typical Application Circuit

Capacitors C1-C6 provide broadband power supply bypassing. C2 and C5 should be tantalum capacitors. All other capacitors should be high quality ceramic capacitors (CK-05 or equivalent).

Adjusting offset

Offset can be broken into two parts; an input-referred term and an output-referred term. The input-referred offset shows up as a variation in output voltage as V_g is changed. This can be trimmed using the circuit in *Figure 3* by placing a low frequency square wave (V_{IN} = 0 to 2V, into V_g with V_{IN} = 0V, the input referred V_{os} term shows up as a small square wave riding a DC value. Adjust R_1 to null the V_{os} square wave term to zero. After adjusting the input-referred offset, adjust R2 (with V_{IN} = 0, V_g = 0) until V_{OUT} is zero. Finally, for inverting applications V_{IN} may be applied to pin 6 and the offset adjustment to pin 3. This offset trim does not improve output offset temperature coefficient.

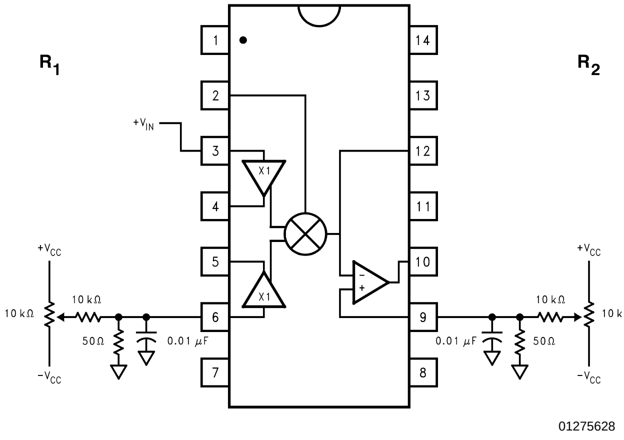


FIGURE 3. CLC520 Offset Adjustment Circuitry (other external elements not shown)

Selecting component values

Most applications of the CLC520 adjust the gain to maximize the V_{OUT} signal. When referred back to the input, this means

Application Information (Continued)

the input signal, signal-to-noise ratio is maximized. The maximum allowed input amplitude and from system specifications, using maximum required gain R_f and R_g can be calculated.

The output stage op amp is a current-feedback type amplifier optimized for $R_f = 1k\Omega$. R_g can then be computed as:

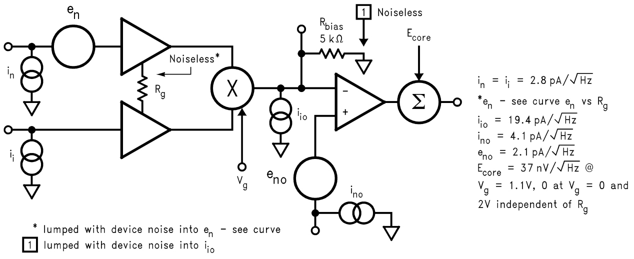
$$R_g = \frac{R_f \times 1.85}{A_{vmax}} - 3.0\Omega \quad \text{with } R_f = 1k\Omega$$

To determine whether the maximum input amplitude will overdrive the CLC520, compute:

$$V_{dmax} = (R_g + 3.0\Omega) \cdot 0.00135$$

the maximum differential input voltage for linear operation. If the maximum input amplitude exceeds the above V_{dmax} limit, then CLC520 should either be moved to a location in the signal chain where input amplitudes are reduced, or the CLC520 gain A_{VMAX} should be reduced or the values for R_g and R_f should be increased. The overall system performance impact is different based on the choice made.

If the input amplitude is reduced, recompute the impact on signal-to-noise ratio. If A_{VMAX} is reduced, Post CLC520 amplifier gain, should be increased, or another gain stage added to make up for reduced system gain..



$i_n = i_i = 2.8\ pA/\sqrt{Hz}$
*e_n – see curve e_n vs R_g
$i_{io} = 19.4\ pA/\sqrt{Hz}$
$i_{no} = 4.1\ pA/\sqrt{Hz}$
$e_{no} = 2.1\ pA/\sqrt{Hz}$
$E_{core} = 37\ nV/\sqrt{Hz}$ @ $V_g = 1.1V$, 0 at $V_g = 0$ and 2V independent of R_g

* lumped with device noise into e_n – see curve
1 lumped with device noise into i_{io}

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FIGURE 4. CLC520 Noise Model

To increase R_g and R_f, where $V_{dmax} = (+V_{IN})-(-V_{IN})$ the largest expected peak differential input voltage. Compute the lowest acceptable value for R_g:

$$R_g > 740\ ^\circ\ V_{dmax} - 3\Omega$$

Operating with R_g larger than this value insures linear operation of the input buffers.

R_f may be computed from selected R_g and A_{VMAX}:

$$R_f = \frac{A_{vmax} \times (R_g + 3.0\Omega)}{1.85}$$

R_f should be $\geq 1k\Omega$ for overall best performance, however $R_f < 1k\Omega$ can be implemented if necessary using a loop gain reducing resistor to ground on the inverting summing node of the output amplifier (see application note QA-13 for details).

Printed Circuit Layout

A good high frequency PCB layout including ground plane construction and power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the Inverting-input (pin12); keep node trace area small. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

For best performance at low maximum gains (A_{VMAX}<10) R_g+ and R_g connections should be treated in a similar fashion. Capacitance to ground should be minimized by removing the ground plane from under the resistor of R_g.

Parasitic or load capacitance directly on the output (pin 10) degrades phase margin leading to frequency response peaking. A small series resistor before this capacitance, effectively reduces this effect (see Settling Time vs. Capacitive Load).

Precision buffed resistors (PRP8351 series from Precision Resistive Products) must be used for R_f for rated performance. Precision buffed resistors are suggested for R_g for low gain settings (A_{VMAX} <10). Carbon composition resistors and RN55D metal-film resistors may be used with reduced performance.

Evaluation PC boards (part no. 730021) for the CLC520 are available.

Predicting the output noise

Seven noise sources (e_n, i_n, i_i, i_{io}, i_{no}, e_{no}, E_{core}) are used to model the CLC520 noise performance (*Figure 4*). e_n, i_n, and i_i model the equivalent input noise terms for the input buffer while i_{io}, i_{no}, and e_{no} model the noise terms for the output buffer. To simplify the model e_n includes the effect of resistor R_g (see *Figure 5* for e_n vs. R_g). To simplify the model further, R_{bias} is assumed noiseless and its noise contribution is included in i_{io}.

An additional term E_{core} mimics the active device noise contribution from the Gilbert multiplier core. Core noise is theoretically zero when the multiplier is set to maximum gain or zero gain (V_g>1.6V or V_g <0.63V respectively at room temperature) and reaches a maximum of 37nV/ $\sqrt{Hz}$ at $A_{VMAX}/2$.

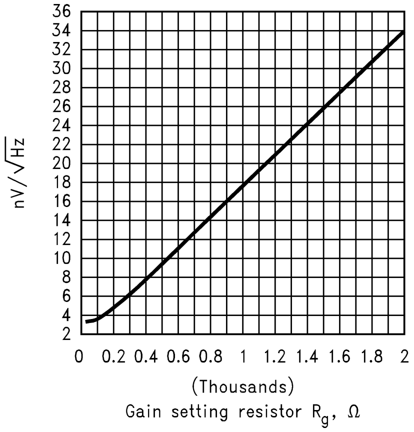

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FIGURE 5. Equivalent Input Noise Voltage (e_n) vs. R_g

Several points should be made concerning this model. First, external component noise contributions need to be factored in when computing total output referred noise. The only exception is R_g, where its noise contribution is already factored in. Second, the model ignores flicker noise contributions. Applications where noise below approximately 100kHz must be considered should use this model with caution. Third, this model very accurately predicts output noise voltage for the typical application circuit (see above) but accuracy will degrade the component values deviate further from those in the typical application circuit. In general, however,

Application Information (Continued)

the model should predict the equivalent output noise above the flicker noise region to within a few dB of actual performance over the normal range of A_{VMAX} and component values.

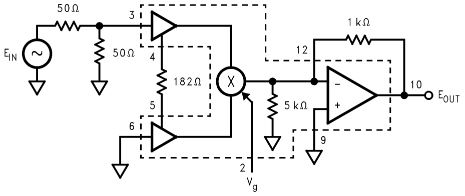

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FIGURE 6. Typical Circuit

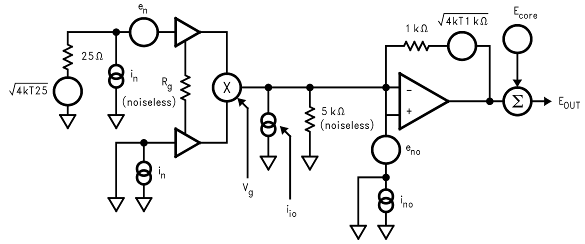

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FIGURE 7. Noise Model for Typical Circuit

Calculating CLC520 output noise in a typical circuit

To calculate the noise in a CLC520 application, the noise terms given for the amplifier as well as the noise terms of the external components must be included. To clarify the techniques used, output noise in a typical circuit will be calculated. (*Figure 6*)

The noise model is depicted in *Figure 7*. The diagram assumes spot noise source with $V_{rms}/\sqrt{Hz}$ and $Amps_{rms}/\sqrt{Hz}$ units. The Thevenin equivalent of the source and input termination is used; 25Ω in series with a noise voltage source. R_g is assumed noiseless since its effect is included in e_n. The internal 5kΩ resistor at the CLC520 core output is also assumed noiseless since its effect is included in i_{io}, The noise contribution from R_f is modeled as a noise source.

The easiest way to analyze the output noise of this circuit is to divide the noise power into three pieces; −input buffer noise calculation, output buffer noise and core noise. The input buffer varies with the gain. The output buffer term is constant. The core noise term is zero at both maximum and minimum gain and reaches peak at $A_{VMAX}/2$.

Since we assume all noise terms are uncorrelated, the equivalent input noise voltage squared is given by:

$$E_{it}^2 = 4kT25 + (I_n 25)^2 + e_n^2$$

i_i does not contribute to the output buffer noise because the input buffer inverting input is grounded. e_n is taken from *Figure 5*.

The equivalent output buffer noise is given by:

$$E_{ot}^2 = (i_{io} \cdot 1k\Omega)^2 + 4kT(1k\Omega) + [e_{no}(1 + \frac{1k\Omega}{5k\Omega})]^2$$

i_{no} does not contribute to the output buffer noise because the output buffer non-inverting input is grounded.

The core noise is already output referred and is $37nV/\sqrt{Hz}$ at V_g =1.1 ($A_{VMAX}/2$) and approaches zero as A goes to 0 or A_{VMAX} Summing the noise power for each term gives the total output noise power.

The total output noise voltage is given by:

$$E_{TOTAL}^2 = E_{it}^2 \; A_V^2 + E_{ot}^2 + C \; E_{core}^2$$

Where A_V is the input to output voltage gain, which varies with V_g.

C accounts for the variation in core noise contribution as V_g is adjusted. C=1 when gain A_V is $A_{VMAX}/2$. C is zero at A_{VMAX} and A_V = 0 and varies between 0 and 1 for all other values.

Using these equations, total calculated output noise for the circuit was $20nV/\sqrt{Hz}$ at minimum gain, $49nV/\sqrt{Hz}$ at mid-gain, and $53nV/\sqrt{Hz}$ at maximum gain.

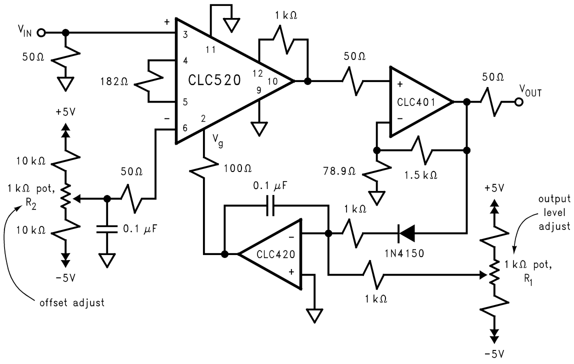

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FIGURE 8. Automatic Gain Control (AGC) Loop

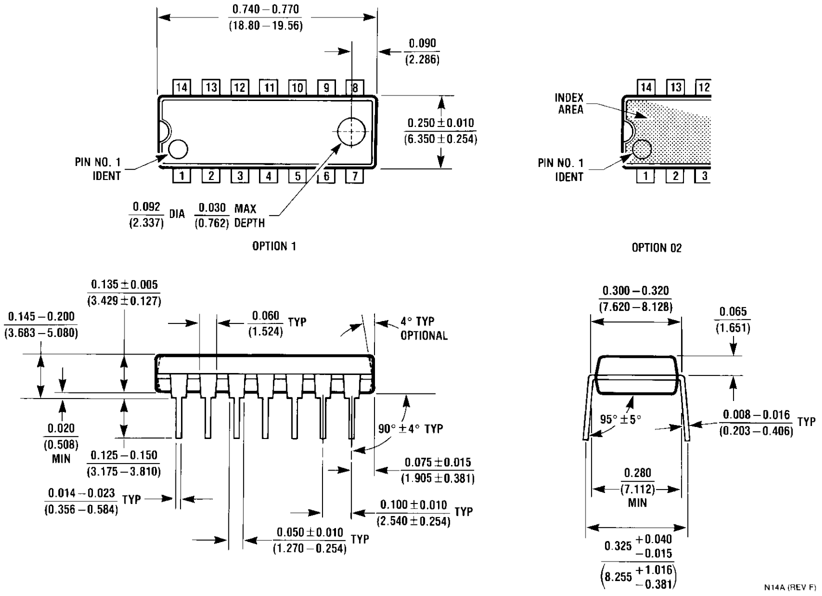
AGC circuits

Figure 8 shows a typical AGC circuit. The CLC520 is followed up with a CLC401 for higher overall gain. The output of the CLC401 is rectified and fed to an inverting integrator using a CLC420 (wideband voltage feedback op amp). When the output voltage, V_{OUT}, is too large the integrator output voltage ramps down reducing the net gain of the CLC520 and V_{OUT}. If the output voltage is too small, the integrator ramps up increasing the net gain and the output voltage. Actual output level is set with R1. To prevent shifts in DC output voltage with DC changes in input signal level, trim pot R2 is provided. AGC circuits are always limited in the range of input signals over which constant output level can be maintained. In this circuit, we would expect that reasonable AGC action could be maintained over the gain adjustment range of the CLC520 (at least 40dB). In practice, rectifier dynamic range limits reduce this slightly.

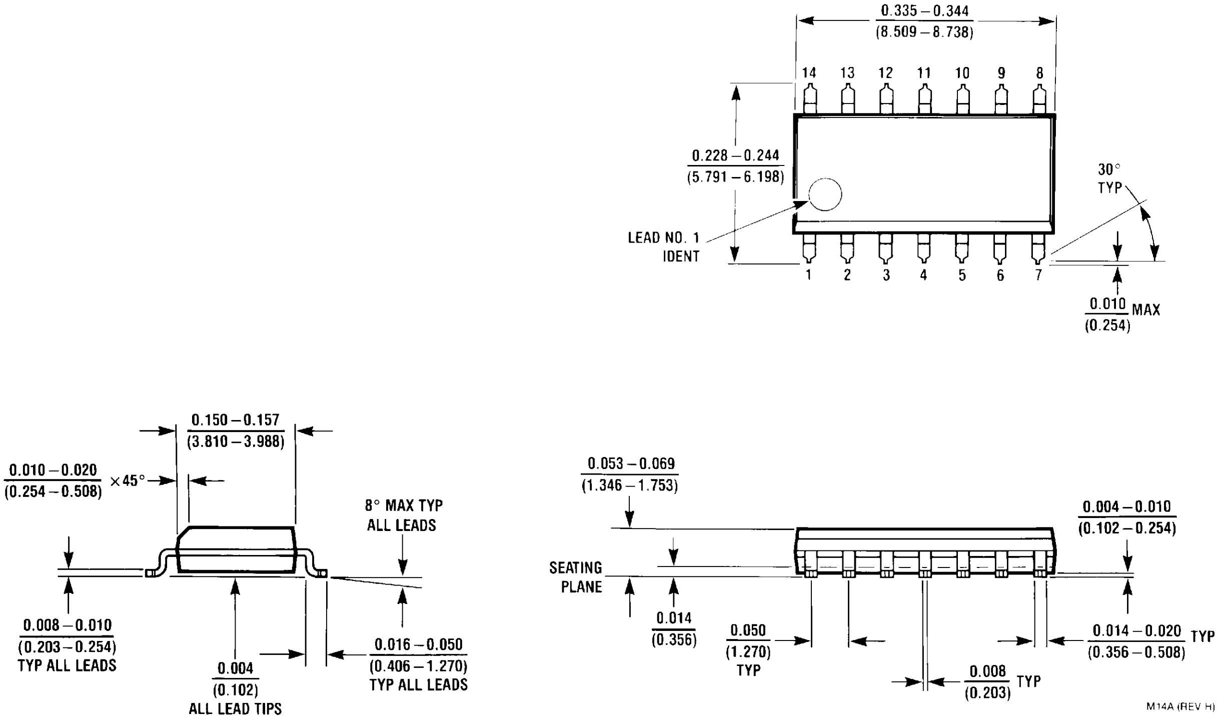
Evaluation Board

Evaluation PC boards (part number 730029 for through-hole and 730023 for SOIC) for the CLC520 are available.

Physical Dimensions inches (millimeters) unless otherwise noted


0.740 – 0.770
(18.80 – 19.56)
0.090
(2.286)
14 13 12 11 10 9 8
1 2 3 4 5 6 7
0.250 ± 0.010
(6.350 ± 0.254)
PIN NO. 1
IDENT
0.092
(2.337)
DIA
0.030
(0.762)
MAX
DEPTH
OPTION 1
INDEX
AREA
PIN NO. 1
IDENT
OPTION 02
0.135 ± 0.005
(3.429 ± 0.127)
0.145 – 0.200
(3.683 – 5.080)
0.060
(1.524)
TYP
4° TYP
OPTIONAL
0.020
(0.508)
MIN
0.125 – 0.150
(3.175 – 3.810)
90° ± 4° TYP
0.075 ± 0.015
(1.905 ± 0.381)
0.014 – 0.023
(0.356 – 0.584)
TYP
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.050 ± 0.010
(1.270 – 0.254)
TYP
0.300 – 0.320
(7.620 – 8.128)
0.065
(1.651)
95° ± 5°
0.008 – 0.016
(0.203 – 0.406)
TYP
0.280
(7.112)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
N14A (REV F)

14-Pin MDIP
NS Package Number N14A


0.335 – 0.344
(8.509 – 8.738)
14 13 12 11 10 9 8
0.228 – 0.244
(5.791 – 6.198)
30°
TYP
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.010
(0.254)
MAX
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
× 45°
8° MAX TYP
ALL LEADS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.008
(0.203)
TYP
0.014 – 0.020
(0.356 – 0.508)
TYP
M14A (REV H)

14-Pin SOIC
NS Package Number M14A

Notes

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